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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,612	04/19/2004	Akihide Shibata	0397-0479PUS1	1186

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,612	SHIBATA ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *8-11 and 21-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 04/19/2004 is acceptable.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/ Restriction

3. Applicant's election of Species I, claims 1-7 and 12-20, in the reply filed on 08/29/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

4. Claims 8-11 and 21-24 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 08/29/2005, as noted above.

Drawings

5. Figures 27-28 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37

CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1-7 and 12-20** are rejected under 35 U.S.C. §103(a) as being unpatentable over Chan U.S. Patent Application Publication 20030005214 (the '214 reference) in view of Yoshikawa U.S. Patent 6,335,554 (the '554 reference).

Chan in the '214 reference discloses a semiconductor memory device in the background art comprising a nonvolatile memory section and a volatile memory section, but fails to teach limitations as claimed for a nonvolatile memory cell for the nonvolatile memory section.

Referring to **claim 1**, the '214 reference discloses a semiconductor memory device comprising:

a nonvolatile memory section (the Flash memory section of the Flash/SRAM package, paragraphs [0004] to [0006], particularly paragraph [0006]); and

a volatile memory section (the SRAM memory section of the Flash/SRAM package, paragraphs [0004] to [0006], particularly paragraph [0006]), wherein

the nonvolatile memory section includes a nonvolatile memory cell.

However, the reference fails to teach that the nonvolatile memory cell includes charge storage areas on both side of a gate of the cell. Specifically, the reference fails to teach that the nonvolatile memory cell having a gate electrode formed on a semiconductor layer via a gate insulating film, a channel region disposed under the gate electrode, diffusion regions disposed on both sides of the channel region and having a conductive type opposite to that of the channel region, and memory functional units formed on both sides of the gate electrode and having a function for retaining charges.

The '554 reference, in disclosing a semiconductor memory device, teaches that a nonvolatile memory cell includes charge storage areas on both side of a gate of the cell so as to store an information corresponding to a plurality of bits in a simple cell structure (paragraph bridging columns 1 and 2). Specifically, the '554 reference teaches a nonvolatile memory cell having a gate electrode (3, Fig. 1) formed on a semiconductor layer (1) via a gate insulating film (2), a channel region (no number) disposed under the gate electrode, diffusion regions (10/11) disposed on both sides of the channel region and having a conductive type opposite to that of the channel region, and memory functional units (4a, 4b) formed on both sides of the gate electrode and having a function for retaining charges (column 6, lines 21+) so as to store an information corresponding to a plurality of bits in a simple cell structure (paragraph bridging columns 1 and 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a prior art semiconductor memory device, such as one disclosed by the 214 reference, such that a nonvolatile memory cell of the nonvolatile memory section includes charge storage areas on both side of a gate of the cell. One would have been motivated to make such a change in view of the teachings in the '554 reference that such a change results in storing an information corresponding to a plurality of bits in a simple cell structure, as detailed above.

Referring to **claim 12**, the '214 reference discloses a semiconductor device comprising:

a semiconductor memory device that comprises:

a nonvolatile memory section (the Flash memory section of the Flash/SRAM package, paragraphs [0004] to [0006], particularly paragraph [0006]);

a volatile memory section (the SRAM memory section of the Flash/SRAM package, paragraphs [0004] to [0006], particularly paragraph [0006]), wherein

the nonvolatile memory section includes a nonvolatile memory cell; and

a logical operation section (such as section 22, Fig. 2, or section 24, Fig. 4) for performing operation processing on the basis of information stored in the semiconductor memory device.

However, the reference fails to teach that the nonvolatile memory cell includes charge storage areas on both side of a gate of the cell. Specifically, the reference fails to teach that the nonvolatile memory cell having a gate electrode formed on a semiconductor layer via a gate insulating film, a channel region disposed under the gate electrode, diffusion regions disposed on both sides of the channel region and having a conductive type opposite to that of the channel

region, and memory functional units formed on both sides of the gate electrode and having a function for retaining charges.

The '554 reference, in disclosing a semiconductor memory device, teaches that a nonvolatile memory cell includes charge storage areas on both side of a gate of the cell so as to store an information corresponding to a plurality of bits in a simple cell structure (paragraph bridging columns 1 and 2). Specifically, the '554 reference teaches a nonvolatile memory cell having a gate electrode (3, Fig. 1) formed on a semiconductor layer (1) via a gate insulating film (2), a channel region (no number) disposed under the gate electrode, diffusion regions (10/11) disposed on both sides of the channel region and having a conductive type opposite to that of the channel region, and memory functional units (4a, 4b) formed on both sides of the gate electrode and having a function for retaining charges (column 6, lines 21+) so as to store an information corresponding to a plurality of bits in a simple cell structure (paragraph bridging columns 1 and 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a prior art semiconductor memory device, such as one disclosed by the 214 reference, such that a nonvolatile memory cell of the nonvolatile memory section includes charge storage areas on both side of a gate of the cell. One would have been motivated to make such a change in view of the teachings in the '554 reference that such a change results in storing an information corresponding to a plurality of bits in a simple cell structure, as detailed above.

Referring to **claims 13 and 14**, similarly as detailed above for claims 1 and 12, the '214 reference discloses s portable electronic apparatus (paragraph [0008], the first few lines

particularly) as claimed and the '554 reference teaches the advantage of the nonvolatile memory cell including charge storage areas on both side of a gate of the cell.

Referring to **claims 2 and 15**, the '214 reference further discloses that the volatile memory section includes an SRAM, as noted above.

Referring to **claims 3 and 16**, the '214 reference further discloses that the nonvolatile memory cell and the SRAM are formed on a single chip ("same package module", paragraph [0006], "chip" is interpreted broadly), as noted above.

Referring to **claims 6 and 19**, the '214 reference further discloses, as noted above, that:

a first chip forming the nonvolatile memory section;

a second chip forming the volatile memory section; and

a single package containing therein the first chip and the second chip (paragraph [0006]).

Referring to **claims 4 and 17**, the '214 reference further discloses that the volatile memory section (as is known in the art) could include a DRAM (paragraph [0004]).

Referring to **claims 5 and 18**, although both the references fail to disclose a refreshing operation means for refreshing the DRAM, a refreshing operation means for refreshing the DRAM is required for the DRAM to function, as is known in the DRAM art.

Referring to **claims 7 and 20**, the '554 reference further teaches that at least a part of the memory functional units (4a or 4b, Fig. 1) overlaps with a part of the diffusion region (10/11).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH TH

Tu-Tu Ho
October 11, 2005